IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:

James M. Derderian

Serial No.: 09/939,258

Filed: August 24, 2001

For: SEMICONDUCTOR DEVICES INCLUDING STACKING SPACERS THEREON, ASSEMBLIES INCLUDING THE SEMICONDUCTOR DEVICES, AND METHODS

Confirmation No.: 2185

Examiner: D. Graybill

Group Art Unit: 2822

Attorney Docket No.: 2269-4831US

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APPEAL BRIEF

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Attn: Board of Patent Appeals and Interferences

Sirs:

This Appeal Brief is being filed in compliance with the requirements of 37 C.F.R. § 41.37(c)(1) and with the fee required by 37 C.F.R. § 41.20(b)(2).

(1) REAL PARTY IN INTEREST

U.S. Application Serial No. 10/939,258 (hereinafter "the '258 Application"), the application at issue in the above-referenced appeal, has been assigned to Micron Technology, Inc., as evidenced by the assignment that has been recorded with the U.S. Patent & Trademark Office (hereinafter "the Office") at Reel No. 012121, Frame No. 0051. Accordingly, Micron Technology, Inc., is the real party in interest in the above-referenced appeal.

(2) RELATED APPEALS AND INTERFERENCES

There are currently no related appeals, interferences, or other actions of which appellants or their attorneys are aware that may have a bearing on the outcome of the decision of the Board of Patent Appeals and Interferences in the above-referenced appeal.

(3) STATUS OF CLAIMS

The '258 Application was filed with fifty-two (52) claims. New claims 53 and 54 were subsequently added.

Of these, claims 2-4, 26, 27, and 36-52 have been canceled without prejudice or disclaimer and claims 9, 24, and 29 have been withdrawn from consideration.

Final rejections have been presented against claims 1, 5-8, 10-23, 25, 28, 30-35, 53, and 54, in the Office Action of November 19, 2007.

(4) STATUS OF AMENDMENTS

Amendments to claims 1, 7, and 9 and the cancellation of claim 6 were proposed in an Amendment Under 37 C.F.R. § 1.116 filed on January 21, 2008. Per the Advisory Action of February 4, 2008, none of these amendments was entered.

(5) SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 1 is drawn to a semiconductor device assembly that includes at least one semiconductor device 30 and at least one resiliently compressible spacer 40. FIG. 1; page 10, line 8, to page 11, line 24 (paragraphs **[0039]** to **[0045]**). The at least one resiliently compressible spacer 40 protrudes from an active surface 32 of the at least one semiconductor device 30 and defines a distance the active surface 32 the at least one semiconductor device 30 is to be spaced apart from a back side 33′ of another semiconductor device 30′. FIG. 1; page 11, lines 3-14 (paragraph **[0044]**).

The semiconductor device assembly of independent claim 28 includes a substrate 20, a first semiconductor device 30, spacers 40, and a second semiconductor device 30′. FIG. 1; page 10, line 8, to page 11, line 24 (paragraphs **[0039]** to **[0045]**). Bond pads 34a of the first semiconductor device 30 communicate with corresponding contact areas 24 of the substrate 20. FIG. 1; page 10, lines 15-23 (paragraph **[0041]**). The spacers 40, which are laterally spaced apart from one another, protrude from an active surface 32 of the first semiconductor device 30. FIG. 1; page 10, line 29, to page 11, line 24 (paragraphs **[0043]** to **[0045]**). At least one of the spacers 40 is in communication with a ground plane or a reference voltage plane of the first semiconductor device 30. Page 10, lines 24-28 (paragraph **[0042]**). That spacer 40 establishes

communication between a back side 33′ of the second semiconductor device 30′, which is positioned on the spacers 40, and the ground plane or the reference voltage plane. Page 14, lines 7-13 (paragraph **[0055]**).

(6) GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

(A) The 35 U.S.C. § 103(a) rejections of claims 1, 5-8, 10-23, 25, 28, 31, 32, 34, 35, 53, and 54 for reciting subject matter that is assertedly unpatentable over the teachings of U.S. Patent 6,724,084 to Hikita et al. (hereinafter "Hikita") and U.S. Patent 6,835,898 to Eldridge et al. (hereinafter "Eldridge"); and

(B) The rejections of claims 16, 30, and 33 under 35 U.S.C. § 103(a) for being drawn to subject matter that is purportedly unpatentable over the subject matter taught in Hikita and Eldridge and, further, in view of teachings from U.S. Patent 6,593,662 to Pu et al. (hereinafter "Pu").

(7) ARGUMENT

Claims 1, 5-8, 10-23, 25, 28, 30-35, 53, and 54 have been rejected under 35 U.S.C. § 103(a).

(A) APPLICABLE LAW

There are several requirements in establishing a *prima facie* case of obviousness against the claims of a patent application. All of the limitations of the claim must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 985 (CCPA 1974); *see also* MPEP § 2143.03. Even

then, a claim "is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art." *KSR Int'l Co. v. Teleflex Inc.*, 82 USPQ2d 1396 (2007). The Office must also establish that one of ordinary skill in the art would have had a reasonable expectation of success that the purported modification or combination of reference teachings would have been successful. *In re Merck & Co., Inc.*, 800 F.2d 1091, 1097 (Fed. Cir. 1986). There must also be "an apparent reason to combine the known elements in the fashion claimed by the patent at issue." *KSR* at 1396. That reason must be found in the prior art, common knowledge, or derived from the nature of the problem itself, and not based on the Applicant's disclosure. *DyStar Textilfarben GmbH & Co. Deutschland KG v. C. H. Patrick Co.*, 464 F.3d 1356, 1367 (Fed. Cir. 2006). A mere conclusory statement that one of ordinary skill in the art would have been motivated to combine or modify reference teachings will not suffice. *KSR* at 1396.

(B) ART RELIED UPON

Hikita

Hikita teaches a semiconductor device with two IC chips 1 and 2 that are electrically connected with front faces 11 and 21, or active surfaces, facing each other. *See, e.g.*, FIG. 10. Bond pads on the active surfaces 11 and 21 of the IC chips 1 and 2 are electrically connected by functional bumps BF1 and BF2 connected to an internal circuit and surrounding the active regions on the IC chips. Col. 11, lines 44-50. Dummy bumps BD1 and BD2 are provided in opposed relation, electrically isolated from the internal circuits on the active surfaces 11 and 21

of the IC chips. Col. 11, lines 50-56. The dummy bumps BD1 and BD2 are positioned to support the central portion of the IC chips. Col. 12, lines 20-26.

Col. 11, lines 50-51, of Hikita confirms the well known fact that the "active surface" of a semiconductor device is the surface on which "functional devices[s]" are formed. As the Office has noted at pages 8 and 9 of the final Office Action, and as is readily understood by those of ordinary skill in the art, the "back side" of a semiconductor device is the surface that is opposite from the active surface. These definitions are consistent with usage of the term "back side" throughout the specification and in the claims of the above-referenced application.

Eldridge

Eldridge teaches resilient electrical contacts that may be used to interconnect terminals of electrical components. Col. 58, lines 41-43. The resilient contacts originate from terminals on a first electrical component and terminate at terminals on another electrical component. Col. 57, lines 45-67. Thus, Eldridge describes resilient contacts bound to a terminal or bond pad on opposing active surfaces of semiconductor dice.

(C) ANALYSIS

(1) HIKITA IN VIEW OF ELDRIDGE

It is respectfully submitted that the teachings of Hikita and Eldridge do not support a *prima facie* case of obviousness against any of claims 1, 5-8, 10-23, 25, 28, 31, 32, 34, 35, 53, or 54.

With respect to the subject matter recited in independent claim 1, it is first submitted that neither Hikita nor Eldridge teaches or suggests an assembly with an active surface of at least one semiconductor device facing the back side of another semiconductor device, let alone an assembly in which at least one spacer defines a distance that the active surface of the at least one semiconductor device is spaced apart from the back side of the another semiconductor device. Instead, the teachings of both Hikita and Eldridge are limited to assemblies in which the active surfaces of two superimposed semiconductor devices face each other. Neither Hikita nor Eldridge suggests that two superimposed semiconductor device may be oriented in any other way.

Second, it is respectfully submitted that, without the benefit of hindsight that the Examiner has enjoyed in examining the above-referenced application, there would have been no motivation for one of ordinary skill in the art to combine teachings from two references that are limited to superimposed semiconductor devices with active surfaces that face one another to develop an assembly in which devices with active surfaces that face in the same direction.

Thus, it is respectfully submitted that a *prima facie* case of obviousness has not been established against claim 1, as is required to maintain a rejection under 35 U.S.C. § 103(a). Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejection of claim 1 is respectfully requested.

Claims 5, 7, 8, and 10-17 are each allowable, among other reasons, for depending either directly or indirectly from independent claim 1, which is allowable.

As for the subject matter to which independent claim 18 is drawn, it is respectfully submitted that neither Hikita nor Eldridge teaches or suggests a semiconductor device assembly

in which the *back side* of a second semiconductor device is positioned on mutually laterally spaced discrete spacers protruding from the active surface of a first semiconductor device. Rather, the teachings of both Hikita and Eldridge are limited to assemblies in which the active surfaces of two semiconductor devices face each other.

Furthermore, since the teachings of Hikita and Eldridge are limited to assemblies in which the active surfaces of two electrically connected semiconductor device face each other, it is respectfully submitted that, without the benefit of hindsight that the above-referenced application provided the Examiner, one of ordinary skill in the art wouldn't have been motivated to combine teachings from Hikita and Eldridge in the manner that has been asserted.

Thus, it is respectfully submitted that a *prima facie* case of obviousness has not been established against independent claim 18, as required to maintain the 35 U.S.C. § 103(a) rejection of that claim. Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejection of independent claim 18 is respectfully requested.

Each of claims 19-23, 25, 28, 31, 32, 34, 35, 53, and 54 is allowable, among other reasons, for depending directly or indirectly from independent claim 18, which is allowable.

(2) HIKITA, ELDRIDGE, AND PU

Each of claims 16, 30, and 33 is allowable, among other reasons, for depending either directly or indirectly from independent claim 18, which is allowable.

Reversal of the 35 U.S.C. § 103(a) rejections of claims 1, 3, 5-8, 10-23, 25, 28, 30-35, 53, and 54 is respectfully requested, as is the allowance of each of these claims.

(8) CLAIMS APPENDIX

Each claim that has been considered in the '381 Application is reproduced in the Claims Appendix to this Appeal Brief.

(9) EVIDENCE APPENDIX

There is no Evidence Appendix to this Appeal Brief.

(10) RELATED PROCEEDINGS APPENDIX

There is no Related Proceedings Appendix to this Appeal Brief.

(11) CONCLUSION

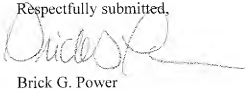
It is respectfully submitted that:

(A) Claims 1, 5-8, 10-23, 25, 28, 31, 32, 34, 35, 53, and 54 are each allowable under 35 U.S.C. § 103(a) for reciting subject matter that patentable over the teachings of Hikita and Eldridge; and

(B) Claims 16, 30, and 33 are allowable under 35 U.S.C. § 103(a) for being drawn to subject matter that is patentable over the subject matter taught in Hikita, Eldridge, and Pu.

Accordingly, it is respectfully requested that the 35 U.S.C. § 103(a) rejections of claims 1, 5-8, 10-23, 25, 28, 30-35, 53, and 54 be reversed, and that each of claims 1, 5-25, 28-35, 53, and 54 be allowed.

Respectfully submitted,



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CLAIMS APPENDIX

1. A semiconductor device assembly, comprising:

at least one semiconductor device; and

at least one resiliently compressible spacer protruding from an active surface of the at least one semiconductor device, the at least one resiliently compressible spacer defining a distance the active surface of the at least one semiconductor device is to be spaced apart from a back side of another semiconductor device to be positioned in superimposed relation with the at least one semiconductor device.

5. The semiconductor device assembly of claim 1, comprising a plurality of spacers that are arranged to stably support the another semiconductor device.

6. The semiconductor device assembly of claim 1, further comprising:

the another semiconductor device positioned adjacent the at least one resiliently compressible spacer, opposite from the at least one semiconductor device.

7. The semiconductor device assembly of claim 6, further comprising:

adhesive material between the at least one semiconductor device and the another semiconductor device.

8. The semiconductor device assembly of claim 7, wherein the adhesive material is located between adjacent spacers.

10. The semiconductor device assembly of claim 1, wherein the at least one resiliently compressible spacer comprises electrically conductive material.

11. The semiconductor device assembly of claim 10, wherein the at least one resiliently compressible spacer communicates with a ground plane of the at least one semiconductor device.

12. The semiconductor device assembly of claim 1, further comprising:
a substrate with which at least one semiconductor device is associated.

13. The semiconductor device assembly of claim 12, wherein the substrate comprises at least one of a circuit board, an interposer, a semiconductor device, and leads.

14. The semiconductor device assembly of claim 12, wherein at least one bond pad of the at least one semiconductor device is in communication with a corresponding contact area of the substrate.

15. The semiconductor device assembly of claim 14, further comprising:
at least one discrete conductive element extending from the at least one bond pad, over an active surface of the at least one semiconductor device, to the corresponding contact area.

16. The semiconductor device assembly of claim 15, wherein heights of the at least one resiliently compressible spacer exceeds a maximum height the at least one discrete conductive element protrudes above the active surface.

17. The semiconductor device assembly of claim 1, wherein the at least one resiliently compressible spacer is secured to noncircuit bond pads of the at least one semiconductor device.

18. A semiconductor device assembly, comprising:

a substrate;

a first semiconductor device associated with the substrate, bond pads of the first semiconductor device in communication with corresponding contact areas of the substrate;

mutually laterally spaced discrete spacers positioned on and protruding from an active surface of the first semiconductor device, at least one spacer of the mutually laterally discrete spacers being in communication with a ground or reference voltage plane of the first semiconductor device; and

a second semiconductor device comprising a back side positioned on the mutually laterally spaced discrete spacers, the at least one spacer establishing communication between the back side of the second semiconductor device and the ground or reference voltage plane.

19. The semiconductor device assembly of claim 18, wherein the substrate comprises one of a circuit board, an interposer, another semiconductor device, and leads.

20. The semiconductor device assembly of claim 18, wherein the bond pads and the corresponding contact areas communicate by way of discrete conductive elements positioned therebetween.

21. The semiconductor device assembly of claim 20, wherein the discrete conductive elements comprise at least one of bond wires, tape-automated bond elements, and thermocompression bonded leads.

22. The semiconductor device of claim 18, wherein the mutually laterally spaced discrete spacers are secured to noncircuit bond pads of the first semiconductor device.

23. The semiconductor device assembly of claim 22, wherein the mutually laterally spaced discrete spacers comprise conductive material.

25. The semiconductor device assembly of claim 23, wherein the mutually laterally spaced discrete spacers are in communication with a ground or reference voltage plane of the first semiconductor device.

28. The semiconductor device assembly of claim 18, wherein at least one of the mutually laterally spaced discrete spacers is compressible.

30. The semiconductor device assembly of claim 18, wherein bond pads of the second semiconductor device communicate with the corresponding contact areas of the substrate by way of discrete conductive elements positioned therebetween.

31. The semiconductor device assembly of claim 18, further comprising:

an adhesive layer between the first semiconductor device and the second semiconductor device.

32. The semiconductor device assembly of claim 31, wherein at least some of the mutually laterally spaced discrete spacers extend through the adhesive layer.

33. The semiconductor device assembly of claim 18, further comprising:

at least one additional semiconductor device positioned over the second semiconductor device.

34. The semiconductor device assembly of claim 18, further comprising:

an encapsulant material substantially covering the first semiconductor device, the second semiconductor device, discrete conductive elements, and portions of the substrate located adjacent to the first semiconductor device.

35. The semiconductor device assembly of claim 18, further comprising:

at least one external connective element carried by the substrate and in electrical communication with at least one corresponding contact area of the substrate.

53. The semiconductor device assembly of claim 1, wherein the at least one resiliently compressible spacer is secured to a contact pad of the at least one semiconductor device.

54. The semiconductor device assembly of claim 18, wherein the at least one spacer is secured to a contact pad of at least one of the first semiconductor device and the second semiconductor device.

EVIDENCE APPENDIX

NONE

RELATED PROCEEDINGS APPENDIX

NONE